Requirements for High Performance RF/UHF ICs and Possible Solutions

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Abstract — **One of the most difficult situations is the operating mode of a base station. As it gets bombarded with signals, it emits a lot of power at the same time. This paper addresses the key problem areas, which are mixers, amplifiers, and oscillators and shows some possible IC-based solutions.**

I. Introduction

Modern handheld communication systems, such as two-way radios and cellphones, always communicate with relay stations or repeaters to extend coverage. The spacing between cells above 400 MHz in average terrain results in a typical coverage of about one mile. This system addresses two markets. One is the handheld device, which is trying to hang on a base station signal and transmit into a base station antenna, and the second is a base station with many pointed antennas that gets bombarded with signals (hostile interference) and transmits into the handheld device. Based on the move to higher frequencies, such as 1800/1900 MHz or even 2.4 GHz, the required number of base stations has exploded. Additional complications occur when many carriers share the same tower and possibly the same antenna system. The dynamic range of both receivers and transmitters has to be quite high and its characteristics are not quite unlike an SSB system requirement. The adjacent channel power requirements are quite stringent, which means that even in a fully saturated system, the system has to maintain a sufficient high dynamic range to accommodate all channels.

The requirements for a chip set for a cellular phone, which is much more complicated than a chip set for a two-way radio, are less problematic since they are less susceptible to interference than a base station. The third order intercept point of a cellphone typically is in the vicinity of –20 dBm, while the desired third order intercept point of a base station is approximately 40 dBm.

As an example, the GSM system has a VCO requirement resulting in a worse case phase noise of –153 dBc/Hz at 800 KHz off the carrier. The same dynamic range has to be obtained by a mixer at a carefully selected gain distribution. Besides the –153 dBc/Hz, the switching time requirements of better than 50μS frequently requires a ping pong arrangement, meaning two synthesizers operating at alternate times.

We have already identified two important building blocks, of which one is the synthesizer, specifically the VCO, and the other being the mixer. In order to obtain the necessary sensitivity or noise figure of typically better than 3 dB, one needs a preamplifier which does not add any intermodulation distortion, improves the system noise figure, and drives the double balanced mixer.

From a technology point of view, we now can choose between gallium arsenide (GaAs) and silicon germanium (SiGe). A 0.35 micron technology for FETs can easily handle mixer circuits, however, for a small insertion loss, a fairly large transistor, like .1μm and 6 fingers, should be used. Difficulties with FET circuits arise from the high impedance, while bipolar transistors, regardless of SiGe or HBTs, have moderate input and output impedances with better matching capabilities. From a linearity point of view, it is still unclear who the winners are. The major drawback of SiGe is the low breakdown voltage. A third class of transistors are now becoming available. They are CMOS devices based on SiGe and Bi-CMOS foundries. I firmly believe the ideal case is a mix of these technologies. High performance mixers with fairly high frequencies of operation should be done in GaAs FET

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technology, while straight forward amplifiers should take advantage of bipolar-based technologies.

We will now look at high performance circuits and discuss how they can be transferred from hybrid technology to RFICs.

II. Block Diagram

Figure 1 shows a level/block diagram of a high performance front end.

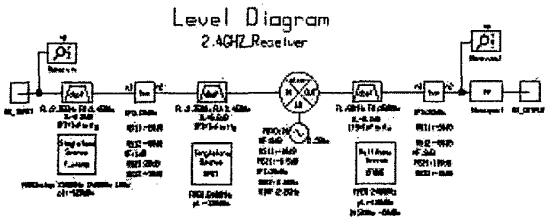

Figure 1. Level diagram of an 2.4 GHz wideband receiver [1].

As mentioned, the critical elements are the preamplifier, the double balanced mixer, a local oscillator system, and the post amplifier driving a stage such as a SAW filter. State-of-the-art mixers vary between 30 and 40 dBm on intercept point and are typically configured as double balanced mixers. The frequency synthesizer typically uses a VCO based on a printed resonator or a ceramic resonator-based design. The amplifier can be either bipolar or field effect transistor type. It appears that bipolar transistors require much more DC current for the same intercept point than FETs. Based on the losses of GaAs or silicon, there is no possibility of designing a filter on the substrate. There is a great need to develop technologies which allow the design of filters without the typical substrate losses. Table 1 shows the resulting intercept points and noise figures of the proposed input stage.

Level Diagram
6GHz Receiver

Calculation of IP_3:

1. Module1: $IP_3 = \infty$
2. Module2: $IP_3 = 23.2dBm = 209mW$
3. Module3: $IP_3 = \infty$
4. Module4: $IP_3 = 31-(-0.2+3.0-0.2) = 31.4Bm = 1380.384mW$
5. Module5: $IP_3 = \infty$
6. Module6: $IP_3 = 140-(-0.2+3.0-0.2-6.0-0.2) = 143.6dBm$
   Input-IP3=2.29086E14mW

$$IP_{3(6Ghz\_Receiver)} = \frac{1}{\sum_{i=1}^{n=6}\left(\frac{1}{IP_3(module)}\right)}$$

$$IP_{3(6Ghz\_Receiver)} = \frac{1}{\frac{1}{\infty}+\frac{1}{209}+\frac{1}{\infty}+\frac{1}{1380.384}+\frac{1}{\infty}+\frac{1}{2.29086E14}} = \frac{1}{0.0055091} = 181.51$$

$IP_{3(6Ghz\_Receiver)} = 181.51mW = 22.58dBm$

Calculation of NF:

1. Module1: NF=0.2dB: F=1.04712
2. Module2: NF=1dB : F=1.2589
3. Module3: NF=0.2dB: F=1.04712
4. Module4: NF=6dB: F=3.98107
5. Module5: NF=0.2dB: F=1.04712
6. Module6: NF=2dB: F=1.58489

$$F_{Total} = F_1 + \frac{F_2-1}{G_1} + \frac{F_3-1}{G_1G_2} + \frac{F_4-1}{G_1G_2G_3} + \ldots\ldots$$

$F = 1.04712 + 0.261 + 0.0001205 + .06 + .01 + 0.054 = 1.4322$

$NF = 1.56dB$

$G_1 \quad G_1G_2 \quad G_1G_2G_3$

$F = 1.04712 + 0.261 + 0.0001205 + .06 + .01 + 0.054 = 1.4322$

$NF = 1.56dB$

III. Discrete Circuits

A. Mixer

While the double-balanced mixer has been used for quite a while, like versions using FETs as diodes as shown in Figures 2 and 3, an FET switching mixer, as shown in Figure 4, has shown very promising results, specifically when arranged in a star mixer configuration. Figure 4 shows a photograph of this mixer built as a prototype using GaAs technology, and Figure 5 shows its schematic. Preliminary tests show an intercept point of 40 dBm and the mixer operates from 700 MHz to 6 GHz with an conversion loss of 9 dB and 2 dB variation over this frequency range. As currently measured, the drive level is +26 dBm, but in reality, a voltage swing of +/- 2V is required. Rather than having an input balun which requires a lot of service area, it would make sense to replace it with LO driver, two stages, so an input drive level of 0 dBm would be sufficient. This is an area of research. The quality of the mixer depends on the accuracy to have an LO drive 180° out of phase.

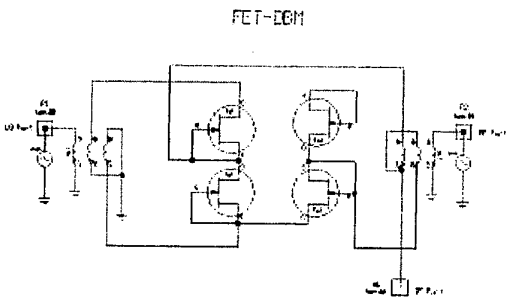

Figure 2. A doubly balanced mixer using GaAs FETs and mixer diodes, gate and source are connected [1, 2].

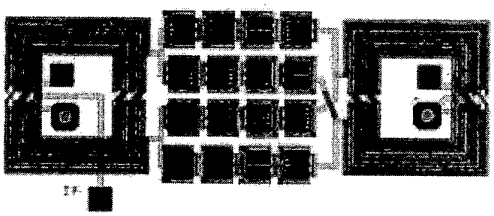

Figure 3. Layout of Figure 2.

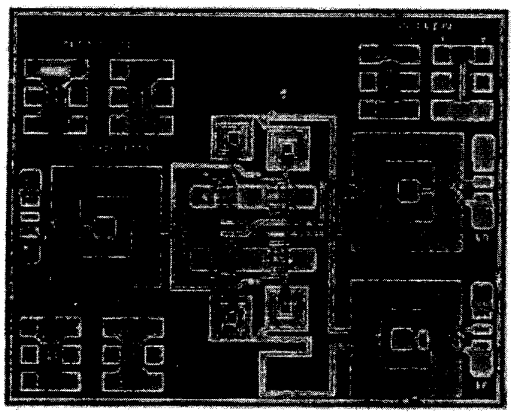

Figure 4. A picture of the Synergy Microwave Corp. passive star mixer using GaAs FET switches.

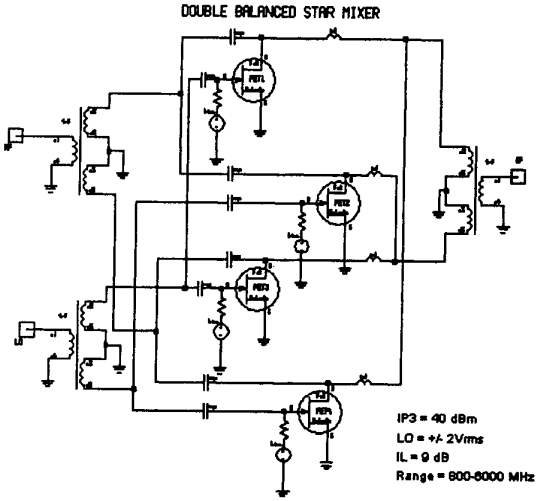

Figure 5. Schematic of the advanced passive star mixer of Figure 4 using GaAs FETs [3].

Figure 6 shows the star mixer with a local oscillator amplifier added. This new approach improves the DC efficiency by 50%.

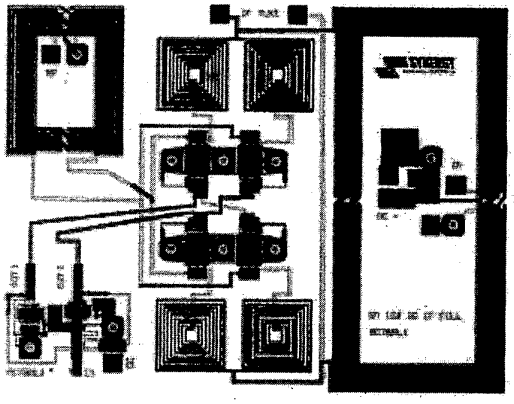

Figure 6. Layout of a proposed star mixer with LO driver.

B. Preamplifier

As mentioned before, the preamplifier and the IF post mixer amplifier significantly contribute to the performance. Figure 7a shows a proposed circuit for a 1 mm FET and a SiGe transistor (Figure 7b). The FET is a good candidate for the IF termination because of its lower

bandwidth, while the SiGe transistor, made by Siemens, is a good candidate for the preamplifier. Unfortunately, the technologies cannot be mixed.

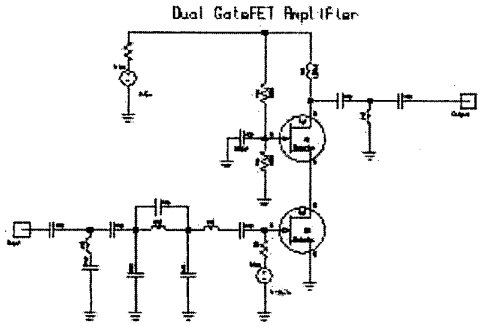

Figure 7a. Cascode circuit using medium power FETS.

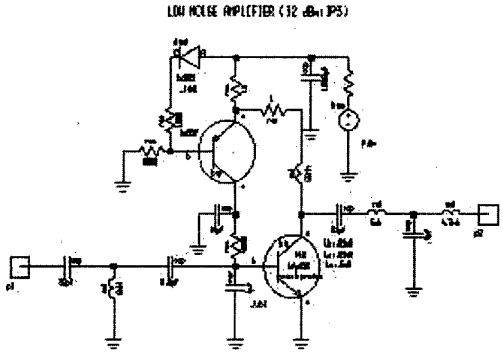

Figure 7b. Low noise, high IP_3 amplifier using a SiGe transistor.

IP_3 = 32 dBm
NF= 1.6 dB
S21 = 25 dB
I_{DC} = 60mA

C. Oscillator

Integrated oscillators are difficult to build because of substrate losses. Figure 8 shows an oscillator that is a candidate for IC implementation. The inductor on the left of the tuning diodes determines the resonant frequency. The transistor feedback circuit improves the phase noise as seen in Figure 9.

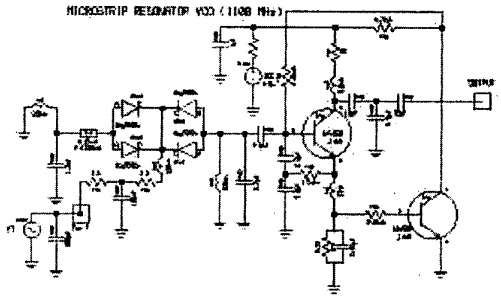

Figure 8. RF Low noise feedback oscillator as a candidate of RF-IC implementation [4].

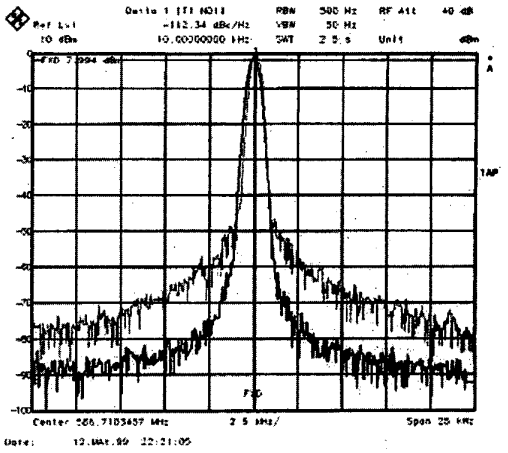

Figure 9. Resulting phase noise improvement from oscillator feedback circuit shown in Figure 8.

In RFIC's, the trend is to go to push/pull oscillators, eliminating the input transformer to the mixer. Figure 10 shows this arrangement. An experimental version of this oscillator is shown in Figure 11, and its phase noise simulation is shown in Figure 12. The actual oscillator circuit layout is shown in Figure 13. Some of the noise problems, due to losses in the substrate, can be cancelled with the feedback, however, research is not finished here.

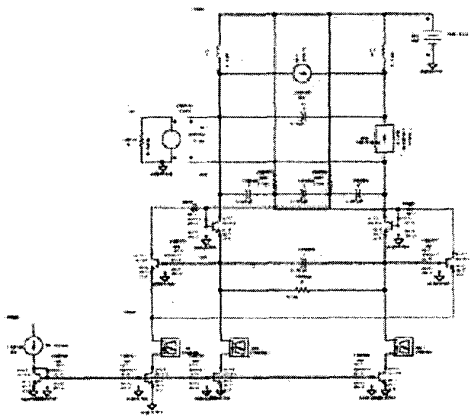

Figure 10. Differential VCO with active flicker noise feedback to reduce phase noise.

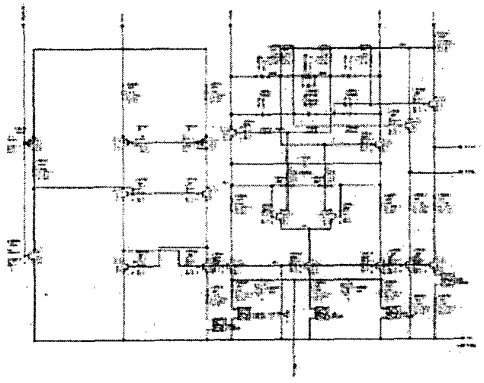

Figure 11. Schematic of the Yellowstone II VCO with active feedback to reduce phase noise.

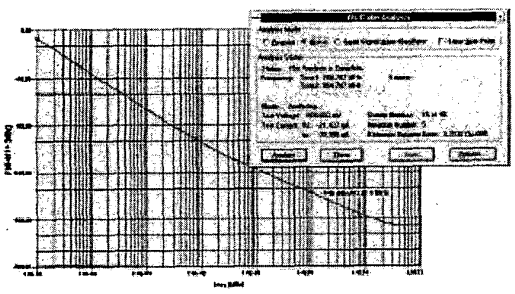

Figure 12. Phase noise simulation of an oscillator.

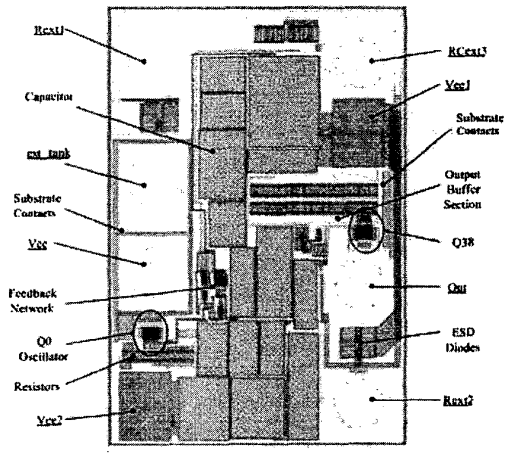

Figure 13. VCO IC layout.

IV. Conclusion

Some high performance stages have been shown which, ideally, should be implemented all on one substrate and on one material. Unless one goes to flip chip arrangements, the ideal candidate would be GaAs FETs/HBTs as a highly integrated arrangement using external inductors. The lack of high Q inductors still limits many designs.

Acknowledgement

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V. References

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[4] Ulrich L. Rohde, "Microwave IC-Based Oscillators," Invited Lecture, Columbia University, December 2000.